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09/868,322	06/18/2001	Yojiro Matsueda	109503	9116

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EXAMINER
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NGUYEN, JENNIFER T

ART UNIT	PAPER NUMBER
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2674

DATE MAILED: 10/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/868,322

Applicant(s)

MATSUEDA, YOJIRO

Examiner

Jennifer T Nguyen

Art Unit

2674

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 18 June 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-26 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

### DETAILED ACTION

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

#### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 5, 6, 9-15, 18-23, 25, and 26 are rejected under 35 U.S.C. 102(b) as being anticipate by Ikeda et al. (U.S. Patent No. 5,815,136).

Regarding claims 1 and 2, referring to Figs. 47A and 47B, Ikeda teaches a display device, comprising: a display drive (2451) having a plurality of scanning lines and a plurality of data lines formed in a grating form corresponding to dots as minimum units of display and active elements provided corresponding to intersections, the display drive (2451) performs display control using a liquid crystal by driving the scanning lines and the data lines; a scanning line driver (2449) that selects and drives the scanning lines, the scanning line driver being allocated corresponding to a length in a column direction of the display drive (2451); a memory (2425) having a plurality of memory cells that are capable of storing an image signal for performing display control of dots in at least one row of the display drive (2451), the memory being allocated corresponding to the length in a row direction of the display drive (2451); a column decoder (2443) allocated corresponding to the length in the row direction of the display drive (2451), the column decoder (2443) selects the memory cells for storing an input-image signal; a

column selection switch section (2445) allocated corresponding to the length in the row direction of the display drive (2451), to switch on the basis of a selection by the column decoder (2443) and the image signal and storing the image signal to said memory cells selected by said column decoder (2443); and a data line driver (2405) allocated corresponding to, the length in the row direction of the display drive, the data line driver drives (2405) said data lines on the basis of the image signal stored in the memory (2425), the data line driver (2405) further being integrated on a semiconductor or an insulating substrate and integrally formed therewith (from col. 31, line 40 to col. 33, line 67 and col. 34, lines 28-65).

Regarding claims 5 and 6, referring to Figs. 47A and 47B, Ikeda teaches a display device, comprising: a display drive (2451) having a plurality of scanning lines and a plurality of bit lines, and a liquid crystal display that is controlled by driving the corresponding scanning lines and bit lines and provided on a dot-by-dot basis as minimum units of display control, and formed in a matrix form; a memory (2425) having a plurality of memory cells that are capable of storing an image signal for performing display control of dots in at least one row of the display drive, the memory (2425) being allocated corresponding to the length in the row direction of the display drive (2451); a column decoder (2443) allocated corresponding to the length in the row direction of the display drive (2451), the column decoder (2443) selects the memory cells for storing an input image signal; and a column selection switch (2445) section allocated corresponding to the length in the row direction of the display drive (2451), to switch on the basis of a selection by the column decoder (2443) and the image signal and storing the image signal to said memory cell selected by the column decoder (2443), the column decoder (2443) being integrated on a

semiconductor or insulating substrate and integrally formed therewith (from col. 31, line 40 to col. 33, line 67 and col. 34, lines 28-65).

Regarding claims 9 and 10, Ikeda further teaches the number of the memory cells, which are allocated corresponding to the length in the row direction of said display drive and capable of storing the image signal for display control of the dots on one row of said display drive, is structured redundantly (col. 33, lines 27-67).

Regarding claims 11 and 12, Ikeda further teaches on the basis of an address signal representative of a display position and a storage position, said scanning line driver selects the scanning lines and the word line driver selects said word lines (Fig. 1A, col. 9, lines 19-67).

Regarding claim 13, Ikeda further teaches independent address signals are inputted to the scanning line driver and the word line driver (Fig. 1A, col. 9, lines 19-67).

Regarding claim 14, Ikeda further teaches the scanning line driver operates to select and drive the scanning lines on the basis of the address signal only when a scanning line driver control signal is inputted, and the word line driver operates to select and drive the word lines on the basis of the address signal only when a word line driver control signal is inputted (Fig. 1A, col. 9, lines 19-67).

Regarding claim 15, Ikeda further teaches the column decoder section (2443) selecting the memory cell to store an inputted image signal on the basis of the address signal (from col. 31, line 42 to col. 32, line 58).

Regarding claim 18, further Ikeda teaches an input interconnection for the image signal to be stored in the memory cell (2425) and the column selection switch section (2445) are formed

on a side opposite to the display drive (2451) sandwiching said memory therebetween (from col. 31, line 40 to col. 32, line 58).

Regarding claims 19-22, Ikeda further teaches the memory (2425) is allocated with the memory cell corresponding to the length in the row direction of said display drive (2451) and formed in a multi-stage structure (from col. 31, line 40 to col. 33, line 67 and col. 34, lines 28-65).

Regarding claim 23, Ikeda further teaches a timing controller (2409) that controls a timing of transmitting the address signal, and a memory controller (2418) that controls the transmitting of the image signal, the memory controller (2418) being integrated on a semiconductor or an insulating substrate and integrally formed therewith (from col. 31, line 40 to col. 32, line 58).

Regarding claim 25, Ikeda further teaches the display drive (2451) and the memory (2425) are directly coupled to supply the image signal comprising a digital signal stored in the memory (2425) to said display drive (2451) (from col. 31, line 40 to col. 32, line 58).

Regarding claim 26, Ikeda further teaches the display drive performs digital drive through area tonal level (from col. 31, line 40 to col. 32, line 58).

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 3, 4, 7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Ikeda et al. (U.S. Patent No. 5,815,136).

Regarding claims 3, 4, 7, and 8, Ikeda teaches all limitations of the claimed invention except fails to teach the display device is organic EL device. However, it would have been obvious to obtain the display device is organic EL device in order to provide a reduction of weight and thickness device with high contrast ratio.

6. Claims 16, 17, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda et al. (U.S. Patent No. 5,815,136) in view of Rao (U.S. Patent No. 5,761,694).

Regarding claims 16 and 17, Ikeda further teaches one pixel displaying as light source, the image signal is inputted on the basis of a unit of one-pixel, and said column decoder selects the memory cell in an amount of one pixel (from col. 17, line 22 to col. 18, line 65).

Ikeda differs from claims 16 and 17 in that he does not specifically teach one pixel comprises three dots provided for developing and displaying red, blue and green. However, Rao teaches pixel comprises three dots provided for developing and displaying red, blue and green (col. 4, lines 60-67). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the pixel comprises three dots provided for developing and displaying red, blue and green as taught by Rao in the system of Ikeda in order to provide a better image display.

Regarding claim 24, Ikeda differs from claim 24 in that he does not specifically teach a D/A converter is provided between the display drive and the memory cell that converts the image signal comprising a digital signal stored in the memory cell into an analog signal, followed by supplying to the display drive. However, referring to Fig. 1A, Rao teaches a D/A converter (106)

is provided between display drive (107) and memory cell (105) that converts the image signal comprising a digital signal stored in the memory cell (105) into an analog signal, followed by supplying to the display drive (107). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the D/A converter is provided between the display drive and the memory cell that converts the image signal comprising a digital signal stored in the memory cell into an analog signal, followed by supplying to the display drive as taught by Rao in the system of Ikeda in order to provide a correspond an analog signal to display image successfully.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kawasaki et al. (U.S. Patent No. 6,223,265) teaches single-chip microcomputer synchronously controlling external synchronously memory.

Sharma et al. (U.S. Patent No. 5,945,974) teaches display controller with integrated half frame buffer and systems and methods using the same.

Motegi et al. (U.S. Patent No. 6,025,822) teaches driving device, a column electrode driving semiconductor integrated circuit.

Kosonocky et al. (U.S. Patent No. 5,361,343) teaches microprocessor system including first and second nonvolatile memory arrays.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Jennifer T. Nguyen** whose telephone number is **703-305-3225**. The examiner can normally be reached on Mon-Fri from 9:00-5:30.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard A Hjerpe** can be reach at **703-305-4709**.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks


Washington, DC. 20231

**Or faxed to: 703-872-9306 (for Technology Center 2600 only)**

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, sixth-floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is 703-306-0377.

Jennifer T. Nguyen  
10/14/2003



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